

ECE 385 Digital Systems Laboratory

Syllabus

Summary:

The goal of ECE 385 course is to teach students design, build, and test/debug a digital system, which can be a 16-bit microprocessor, a dedicated logic core, or a system-on-a-chip (SoC) platform. Students will learn about the modular design approach, which is the underlining principle of IP-based SoC design methodology. Students will start with discrete logic in the first labs to strengthen their skills of using physical logic elements to build relatively complex circuits such as a 4-bit serial processor. Then, the course will make a transition to SystemVerilog and RTL design methodology. The concept of modular design is carried over to SystemVerilog so students would have a concrete understanding of the connection between wired circuits on the proto-board and mapped circuits on the FPGA board, and the RTL design abstraction can be better captured through this process. Students will then start to gradually learn how to design and realize digital circuits using SystemVerilog and the FPGA board. These labs would include 8-bit serial processor, arithmetic units, 16-bit SLC-3 processor, USB input and HDMI display, and a simple SoC that connects a MicroBlaze embedded processor with a custom AXI4 display controller. Finally, students will have four weeks at the end of the semester to work on an open project of their own choice based on FPGA design with SystemVerilog. This open final project will be graded by creativity, complexity, and functionality of the design.

Learning Objectives:

Students will learn about combinational and sequential logic, storage elements, I/O and display, timing analysis, design tradeoffs, synchronous and asynchronous design methods, data-path and controller design, microprocessor design, software/hardware co-design, system on chip design and operation, simulation, digital systems testing, and FPGA EDA (electronic design automation) tools.

Prerequisites: ECE 120, ECE 220 (or CS 225)

Credits: 3

Lecture meeting times and location: M/W 4:00-4:50pm; 1002 ECEB

Lab location: TBA

Instructors: Prof. Zuofu Cheng

Office Hours: (posted on website)

Course website: <http://courses.engr.illinois.edu/ece385>

Course Materials:

- Lab manual (ECE 385 Lab Manual – found online at <http://courses.engr.illinois.edu/ece385>)

- ECE 385 Laboratory Kit - order from <https://ece.illinois.edu/academics/ugrad/lab-kits>
- Real Digital “Urbana” FPGA development board (one checked out per student)
- Reference books (ECE 120 textbook, others on reserve at Grainger)

Course Topics and Laboratory Assignments:

#	Name	Short Description
1	Introductory Discrete Logic Experiment	Introductory discrete logic experiment, students will build simple 2:1 MUX and understand effect of glitches on combinational logic. Students will also review principles of digital circuit construction with discrete integrated circuits, reviewing combinational and sequential logic, K-maps, debouncing, etc.
2*	A Logic Processor	Students will design and construct a 4-bit serial logic processor using discrete logic and demonstrate the assignment to the section TA. Students will review finite state machine design techniques, learn about Mealy and Moore state machines, and construct their circuit. Students will be provided a version of their design in SystemVerilog, which they will extend to 8 bits and test on the FPGA board and in simulation.
3	16-bit Adders in SystemVerilog	Students will learn about 3 different kinds of combinational adders and their running times and tradeoffs. They will then construct each adder on the FPGA using SystemVerilog, and evaluate the relative performance, area, and power efficiency. The lab will introduce students to combinational logic design using the FPGA and SystemVerilog, as well as the design statistics and other analysis tools provided by the Vivado EDA suite.
4	An 8-Bit Multiplier in SystemVerilog	Students will construct an 8x8 to 16-bit serial multiplier in SystemVerilog and test on the FPGA. They will review 2’s complement numbers and learn sequential and FSM design on the FPGA.
5*	Simple Computer SLC-3.2 in SystemVerilog	Students will design and construct a 16-bit CPU based on a simplified version of the LC-3 ISA they learned in previous courses (SLC-3). Students will demonstrate their CPU running a series of provided test programs, including software multiply and sort functions. In addition to the construction of the CPU and familiarization with SystemVerilog, students will learn about the on-chip memory blocks on the FPGA. They will be tasked with debugging a complex design using both simulation tools and hardware tools such as the Vivado debug cores.
6*	SoC with USB and HDMI	Students will follow a tutorial and instantiate a system-on-chip project using the MicroBlaze embedded processor core. They will configure the memory spaces and peripherals using Platform

		Designer and write a simple test program demonstrating the functionality of their system. They will then modify their platform to add a SPI peripheral – which they will then use to connect the MicroBlaze processor to a USB transceiver to create a USB host system for an external keyboard or mouse. Students will test their code by instantiating some provided modules, which display a bouncing ball to be controlled by the keyboard and/or mouse.
7*	SoC with HDMI Display Controller	Following a tutorial, students will create an AXI bus peripheral for hardware software data exchange. They will then design and construct a hardware display controller based on the provided content from the previous lab. For the first week, students will create an IP which can display 80x30 text on the HDMI monitor controlled via the CPU. For the second week, students will modify their design to support color via a palette.
FP	Final Project	See grading section and course website for detailed requirements and suggestions for projects.

Labs marked with an asterisk (*) denote 2-week labs.

Grading policy:

- 7 Experiments (175 points):
 - Lab 1 is report only (15 points)
 - Lab 2, 5, 6, 7 are 2-week assignments with (10 demo points each and 20 lab report points)
 - Labs 3 and 4 are 1-week assignments with 5-point demos and 15-point reports
 - Individual functional tests for the demo points are found on the course webpage.
 - Each lab assignment includes a checklist for the lab manual; **however, lab reports must be written coherently into sections and paragraphs, rather than simply be a collection of data and answers to questions.**
- 10 Quizzes (60 points):
 - 6 points each, for students working in groups see **Partnership** section for the distribution.
- Final Project (60 points):
 - Functionality (20 points)
 - Functionality points are allocated towards completeness and the correct operation of your proposed design.
 - 5 points are allocated for the mid-checkpoint. This is largely graded based on attendance to the mid-checkpoint and satisfactory progress. Satisfactory progress means that you have largely finished your research phase and have some code to demonstrate.
 - 15 points are allocated for the final demo. If your circuit meet the fundamental requirements of your proposed circuit (discuss with TA), you will most likely receive close to full credit. If your circuit meet most of the fundamental requirements but is lacking some minor details or if the

circuit is glitchy/buggy, you will most likely receive more than half of the credits. If your circuit is lacking fundamental requirements or if little physical demo is shown other than the written codes, you will most likely receive less than half of the credits. Note that if you demo a project significantly different than your proposal, you may receive fewer functionality points if what you demo was significantly easier than what you proposed.

- Difficulty (10 points)
 - 10 points are allocated towards the intrinsic difficulty of your proposed design. That is, the complexity of your design/logic/state machine/algorithm inherent to the choice of your project. Note that this may include both technical difficulty and usability difficulty (e.g. points may be deducted for a game which has poor responsiveness or poor framerate). Also, keep in mind that some approaches to similar functionality may have different difficult levels (e.g., score keeping on the HEX displays is easier than score keeping on the VGA display using font drawing). Ideas to add difficulty can include:
 - Addition of sound/speech
 - Score keeping in game/font drawing/high score table.
 - Multiplayer in game
 - AI
 - External hardware
 - Live video
 - Sophisticated graphics drawing
- Proposal and Final Report (30 points)
 - 10 points are allocated towards your project proposal. This is an example of what a good proposal should include (.PDF link). A good proposal showing sufficient feasibility research is the first step to a good final project. Uploaded to Compass during project week 0, same due time as the final lab report.
 - 20 points are allocated towards the final report. The proposal may be a good outline to start the final report from, but the final report should also include all the sections as in the previous 7 lab reports the Wednesday after the Final Demo.
- Peer Evaluation (5 points):
 - Five distributed 1-point peer evaluations throughout the semester.

Total points: 300, standard grading scaling e.g. >97.00% A+, >93.00% A >90.00% A-

Students should note that although a lab demonstration may be worth 10 points, most labs have functional demos broken down into 10 smaller functionality tests worth 1 point each, with a large comprehensive test (worth the total amount, to save on demo time). For example, the 16-bit CPU has a SORT test worth 7 points, but students who cannot get the SORT test to function may demo a simpler test for partial credit.

Lab Policies:

Each week, students are to sign up for a lab demonstration section. During this session, students are to demonstrate the functionality of the circuit to their section TA using a combination of **screen share** and **webcam**. Certain labs (for example, the TTL design) must be demonstrated to the TA **in-person**. The website of the current lab will list the expected functionality of each aspect of the design and the corresponding grade weight. Students are also required to take an oral quiz with randomized questions relevant to the current lab. The quiz is delivered **like that of a technical interview**, TAs ask the quiz question to the students and the students are expected to give a reasonable response **while on camera**. Students may ask clarifying questions to the TA and are allowed to ‘think through’ their answer (within reason, typically about 3 minutes per question). **Demo sessions are recorded to allow for review of any disputes regarding demo points or quiz grading.**

Partnership:

Students are allowed to work in groups of up to 2. This requires that both partners be present in each demo and demo simultaneously. Grades for the lab demos, reports, and the final project will then be shared by each partner. Both partners will be independently given a different question for the quiz. To foster a sense of shared responsibility, each quiz question will be worth up to 4 points for the student receiving the question, and up to 2 points for the lab partner. Students who choose to work alone may do so, they will be solely responsible for 2 quiz questions (with their better answer being worth more). **Partnerships may be dissolved and formed at the discretion of each student, provided students notify the partner and the TA a week in advance. Students who feel that their lab partners are not contributing to the partnership should be free to find another partner or work solo. Partners are required to fill in a peer evaluation at five points throughout the semester. Each peer evaluation is worth 1 point for a total of 5 points and will be anonymous to the other partner.**

Resources:

Students will be responsible for attending lectures in person or by watching the recordings, working on the laboratory assignments asynchronously, writing their lab reports, and signing up for demos and taking oral quizzes. To assist students, the course has a join Campuswire bulletin board where students may ask questions and help peers. Course staff will monitor Campuswire and try to answer questions as they come up. **In addition, we have many undergrad assistants who will hold open lab office hours (typically in 3022 ECEB). This will be the primary way in which students will obtain personalized help in completing the laboratory assignments.** Notice that students are responsible for putting themselves in the queue and asking useful questions – the undergraduate assistants are instructed to answer questions and help students but

will not give out answers on explicitly how to do the labs. The instructor will also hold office hours (one hour weekly, longer if necessary) to answer questions.

The instructor will also hold a **Friday Q/A session**. The Q/A session will use a live-stream format and is intended as a casual check in and debriefing session after the student's Friday demo. Students can also ask questions about the next lab and suggest course improvements in a casual setting. The final Friday Q/A check-in will consist of a project showcase of impressive final projects. Prof. Cheng will try to get projects that students sent him to run and demonstrate them to the rest of the class.

Accommodations:

Students who have DRES letter of accommodations should contact Prof. Cheng at the beginning of the semester and work with Prof. Cheng to satisfy those accommodations. All students are expected to substantially complete the same laboratory assignments and satisfy the same learning objectives, but accommodations may be provided in the form of extensions and extra time on the quizzes as appropriate according to DRES. Students who have undiagnosed disabilities should seek a DRES evaluation as soon as possible, though accommodations may be given on a case-by-case basis if (for example) the student is undergoing evaluation but cannot receive a letter in time.

As there are constant stream of assignments, there is no formal late policy. Students who miss assignment deadlines due to procrastination are encouraged to work on the current lab to avoid falling behind permanently. Students who have excused absences (illness, death in family, job interviews, etc.) must contact and work with Prof. Cheng to set extended deadlines working around their absence.