Syllabus: ECE 462

Logic Design and Synthesis

Fall 2025

Course Director: Prof Shobha Vasudev

Instructor: Anu Aggarwal (agganu@*illinois.edu*)
Class Meetings: MWF, 10-10:50 am **(ECEB 3013)**
Office hours (ECEB 3044): TBD.

Course Staff:
TA: Wesley Wu, Anay Koorapaty
Graders: Daniel Vlassov

Textbook:

Logic Synthesis and Verification Algorithms by Hatchel and Somenzi
https://link.springer.com/book/10.1007/b117060

Grading:

- Homework assignments: 20%
- Class participation (Quizzes/attendance/other): 15%
- Exams (2Midterms & Final): 15%, 20%, 30%
- Extra credit project – 10% of overall grade.

Lecture slides and recordings: Lecture slides will be available on canvas. Recordings will be available on the Illinois media space.

Grades: Grades will be posted to Canvas for canvas based assignments.

Homework: will be submitted and due electronically via Canvas. HW due dates (normally Mondays) will be mentioned on the HW. Homework can be submitted up to 2 days late with penalty of 10% grade reduction per day except for the last HW as it will be immediately before the final exam. Solutions will be posted on canvas after the late due date. Regrade requests can be submitted on canvas up to a week after the grade release.

In class worksheets: will be submitted electronically via Canvas. In-class worksheets will be group activities. Each person will have to submit a separate worksheet to the canvas by midnight the day after it is assigned. One of these will be picked by graders for grading. Entire group will receive the same grade as the graded assignment. Grade will be assigned for best of 90% of the worksheets.

Past exam samples: will be available on canvas a week before the exam.

Learning Objectives:

1. Know about various algorithms used in synthesis as means to do layout from Verilog.
2. Be able to use Quine McCluskey, branch and bound, unate cover, heuristic methods in addition to K-maps and the principles of Boolean algebra for Boolean function optimization.
3. Know how to minimize multiple output functions using various algorithms.
4. Can build binary decision diagrams and use them in VLSI design.

5. Can optimize FSMs.
6. Understands how ATPG works and can design for test.
7. Knows why multiple level functions are required and how to optimize them for synthesis.
8. Understands the importance of technology mapping in synthesis (if covered) and can chose appropriate parameters/technology for a design.

Tentative Schedule

Week	Topic	Readings
1	Introduction to Logic Design and synthesis	1.1.1-1.4.4
	Boolean Algebra	3.1.1-3.1.3, 3.2.1, 3.2.5
2	Boolean Algebra	3.2.6, 3.3.3-3.3.4, Theorem 3.2.10& 3.2.11
	Karnaugh maps	4.3
3	Quine McClusky	4.4, 4.5
	Quine McClusky	4.4, 4.5
4	Unate covering problem, dominance, Heuristic Methods	4.6, 4.7, 4.8.1-4.8.4
	Branch and bound method	4.8.5
5	Branch and bound method	4.9
	Branch and bound method	4.9
6	*Midterm 1*	
	Multiple Output functions	4.10
7	Function Classification	5.1, 5.2.1
	Function Classification	5.1, 5.2.1
8	Function Classification	5.2, 5.2.2, 5.2.3, 5.3
	Binary Decision Diagrams	Chapter 6.1
9	*Spring break*	
10	Binary Decision Diagrams	Chapter 6.2-6.3
	Binary Decision Diagrams	Chapter 6.3
11	Finite State Machines	Chapter 7.3.1
	Finite State Machines	Chapter 7.4
12	Finite State Machines	Chapter 7.7.5
	Midterm 2	
13	Finite State Machines	Chapter 7.8
	Automatic Test Generation	Chapter 12.1-12.3.1
14	Automatic Test Generation	Chapter 12.3.2-12.4
	Automatic Test Generation	Chapter 12.3.2-12.4
15	Multilevel Logic Synthesis	Chapter 10.1, 10.2.2, 10.4, 10.5
	Multilevel Logic Synthesis	Chapter 10.3, 10.5
16	Multilevel Logic Synthesis	Chapter 10.7
Exams	*Final Exam week*	Cumulative