ECE 427/498HK - Advanced VLSI System Design

Course Staff
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Office Hour(s): *see schedule on Canvas*

Course Description
Students will work in teams on a semester-long project to design and fabricate their own digital, analog, or mixed-signal chip using modern EDA tools. Each team will propose a design in the form of specifications, write an RTL (or equivalent) model for their chip and its components, design schematics, create a testing/debug strategy, and perform layout, integration, and verification of their chip. Final GDS files will be sent to foundry at the end of semester.

Course Prerequisites
ECE 425. (ECE 411 Recommended. ECE 482 and 483 Required for Analog Projects.)

Major Assignments
- **Project Proposal** – Proposal document and presentation describing the project's goals, high-level design, task division, and timeline. Due on the second week of class.
- **Midterm Report** – Progress report documenting completed designs, verification coverage, schematics and layouts done halfway through the semester. Digital projects are expected to complete RTL design by this deadline.
- **Trial GDS** – Trial GDSII file handed to MPW partner for initial design rule checks, students will have a chance to fix violations after getting feedback from foundry.
- **Final GDS** – Final GDSII file handed to MPW partner, and subsequently to foundry for tapeout. Accompanying specifications and DRC waivers must also be completed.
- **Final Report** – Final project report in IEEE conference paper style documenting the entire design, specifications, verification and test strategies, and challenges faced throughout the entire project.

Important Deadlines for Fall 2024
Trial GDS – 11/13/2024
Final GDS – 11/20/2024

Late Assignment Policy
Late assignments may be submitted within 24 hours of the deadline at a 10% grade penalty, this applies only to written assignments (reports). Trial and Final GDS deadlines are exact with no extensions allowed (we must adhere to foundry deadlines).

Reference Texts
- *CMOS VLSI Design: A Circuits and Systems Perspective* by Harris and Weste.
- *Digital Integrated Circuit Design Using Verilog and SystemVerilog* by R. W. Mehler.
- *SystemVerilog for Verification* by Chris Spear.
- *VLSI Test Principles and Architectures: Design for Testability* by Cheng-Wen Wu.

Course Schedule

Date	*Lecture*	*Expected Project Timeline*
08/27/2024	Course Introduction	**Environment Setup**
09/03/2024	Project Proposal Presentations	**Hardware Design Phase**
09/05/2024	**ASIC Design Workflow**	
09/12/2024	**EDA Software Tutorial**	
09/19/2024	**Writing Synthesizable RTL**	
09/26/2024	Group Progress Review	
	Memories and IPs	
10/01/2024	**Design Verification (I)**	
	|- SystemVerilog Assertions	
10/03/2024	**Design Verification (II)**	
	|- Advanced Testbench Features	
10/10/2024	**Hardware Synthesis (w/ Design Compiler)**	
	|- Synopsys DC In-depth Tutorial	
	|- Multiple Clock Domains	
10/15/2024	**Midterm Progress Review**	**RTL Freeze / Midterm Report**
10/17/2024	**Physical Implementation (I)**	**Physical Design Phase**
	|- Floorplanning and Power Planning	
10/22/2024	**Physical Implementation (II)**	
	|- Clock Tree Synthesis	
	|- Place and Route Optimizations	
10/29/2024	**Physical Implementation (III)**	
	|- Static Timing Analysis	
	|- Parasitic Extraction	
10/31/2024	**Pre-Silicon Validation (I)**	
	|- DRC and LVS	
11/05/2024	Group Progress Review	
	Pre-Silicon Validation (II)	
11/12/2024	*Office Hours*	
11/13/2024	**Trial GDS Handoff**	**Trial GDS Due**
11/19/2024	*Office Hours*	
11/20/2024	**Final GDS Handoff**	**Final GDS Due**
11/26/2024	*Fall Break*	
11/28/2024	**Special Topics**	
12/03/2024	**Special Topics**	
12/10/2024	**Project Presentations**	**Final Report**

Note: Special topics and guest lectures may vary by semester.

Weekly Progress Meetings

In addition to the midterm and final progress reports, there will be two minor group progress reviews in-class on 9/26 and 11/5. Furthermore, each group is required to meet with course staff every week to discuss their progress. We recommend that all group members attend but exceptions can be made if scheduling is difficult. Further instructions can be found on Canvas.

Grading Breakdown

ECE 427/498HK Grading Policy

Percentage	Assignment	Description
10%	Attendance / Progress Reviews	Attend lectures and weekly progress meetings. ▪ 2% In-class lecture attendance. ▪ 4% Four progress reviews and evaluations. ▪ 4% Weekly office hours attendance (group).
5%	Project Proposal	Proposal document and presentation (due week 1). ▪ 4% Proposal satisfies all criteria indicated on Canvas. ▪ 1% Proposal presentation.
10%	Mid-Term Report	Written mid-semester progress report (due week 8). ▪ 3% Report satisfies all mid-term report criteria. ▪ 5% Completed RTL design according to timeline. ▪ 2% Individual contribution.
10%	Final Presentation	Oral final presentation (week 16). ▪ 3% Presentation clarity and member attendance. ▪ 2% Answers to instructor and student questions. ▪ 5% Quality of final design based on specifications.
15%	Final Report	Written final report (week 16). ▪ 2% Design documentation. ▪ 3% Accomplished features relative to proposal. ▪ 5% Individual contribution. ▪ 5% Final GDS submission.
50%	Project Completion	Final design and physical implementation (week 16). ▪ 10% Completed RTL design and verification. ▪ 10% Completed synthesis and submitted netlist. ▪ 10% Completed physical implementation. ▪ 20% Individual contributions to project.

[Note] The project is done in groups of 4-6 students.

Grading Scale

Note that the letter grade scale provided below may be adjusted based on the class average.
A > 92%, **A-** > 88%, **B+** > 84%, **B** > 80%, **B-** > 75%, **C** > 60%, **D** > 50%, **F** < 50%.

Acknowledgements

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